



FORM PTO-1449		ATTY. DOCKET NO. 1875.0560001/RES/AJF		APPLICATION NO. 09/844,432				
INFORMATION DISCLOSURE STATEMENT		APPLICANTS BUCHWALD et al.				FILING DATE April 30, 2001		GROUP 2681
U.S. PATENT DOCUMENTS								
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE	
JP	AA1	5,485,490	01/1996	Leung et al.	375	371	11/29/1994	
JP	AB1	5,757,857	05/1998	Buchwald	375	271	07/21/1994	
JP	AC1	6,122,336	09/2000	Anderson	375	371	09/11/1997	
	AD1							
	AE1							
	AF1							
	AG1							
	AH1							
	AI1							
	AJ1							
	AK1							
FOREIGN PATENT DOCUMENTS								
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION	
	AL1						Yes No	
	AM1						Yes No	
	AN1						Yes No	
	AO1						Yes No	
	AP1						Yes No	
OTHER (Including Author, Title, Date, Pertinent Pages, etc.)								
	AR	1						
	AS	1						
	AT	1						
EXAMINER <i>Jan He</i>					DATE CONSIDERED <i>6/30/04</i>			
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.								



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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
JP	AA1	5,485,490	01/1996	Leung et al.	375	371	RECEIVED JUL 24 2002 Technology Center 2000
JP	AB1	5,650,954	07/1997	Minuhin	364	825	
JP	AC1	5,881,108	03/1999	Herzberg et al.	375	296	
JP	AD1	5,966,415	10/1999	Bliss et al.	375	35	
JP	AE1	6,002,279	12/1999	Evans et al.	327	144	
	AF1						
	AG1						
	AH1						
	AI1						
	AJ1						
	AK1						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
JP	AL1	0 483 439	05/1992	PCT	H04L	25/03	Yes No
JP	AM1	EP 0 515 074	11/1992	PCT	H03L	7/099	Yes No
JP	AN1	EP 0 805 447 A2	11/1997	PCT	G11B	20/10	Yes No
JP	AO1	EP 0 909 035	04/1999	PCT	H03L	7/08	Yes No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

JP	AR	<u>1</u>	Buchwald, A. and Martin, K., "Integrated Fiber-Optic Receivers," Kluwer Academic Publishers, 1995 (entire book submitted).
JP	AS	<u>1</u>	Sidiropoulos, S. and Horowitz, M., "A Semidigital Dual Delay-Locked Loop," IEEE Journal of Solid-State Circuits, IEEE, Vol. 32, No. 11, November 1997, pp. 1683-1692.
JP	AT	<u>1</u>	Copy of International Search Report issued January 24, 2002, for Appln. No. PCT/US01/13613, 7 pages.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA2						
	AB2						
	AC2						
	AD2						
	AE2						
	AF2						
	AG2						
	AH2						
	AI2						
	AJ2						
	AK2						

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JUL 29 2002
Technology Center 2681**FOREIGN PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
	AL2						Yes No
	AM2						Yes No
	AN2						Yes No
	AO2						Yes No
	AP2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

JP	AR	2	Copy of International Search Report issued April 11, 2002, for Appln. No. PCT/US01/13637, 2 pages.
	AS	2	
	AT	2	

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